

# MC100E337

## 5V ECL 3-Bit Scannable Registered Bus Transceiver

The MC100E337 is a 3-bit registered bus transceiver with scan. The bus outputs (BUS0–BUS2) are specified for driving a 25 Ω bus; the receive outputs (Q0 – Q2) are specified for 50 Ω. The bus outputs feature a normal HIGH level ( $V_{OH}$ ) and a cutoff LOW level – when LOW, the outputs go to –2.0 V and the output emitter-follower is “off”, presenting a high impedance to the bus. The bus outputs also feature edge slow-down capacitors.

Both drive and receive sides feature the same logic, including a loopback path to hold data. The  $\overline{HOLD/LOAD}$  function is controlled by Transmit Enable (TEN) and Receive Enable (REN) on the transmit and receive sides respectively, with a HIGH selecting LOAD. Note that the implementation of the E337 Receive Enable differs from that of the E336.

A synchronous bus enable (SBUSEN) is provided for normal, non-scan operation. The asynchronous bus disable ( $\overline{ABUSDIS}$ ) disables the bus immediately for scan mode.

The  $\overline{SYNCEN}$  input is provided for flexibility when re-enabling the bus after disabling with  $\overline{ABUSDIS}$ , allowing either synchronous or asynchronous re-enabling. An alternative use is asynchronous-only operation with  $\overline{ABUSDIS}$ , in which case  $\overline{SYNCEN}$  is tied LOW, or left open.  $\overline{SYNCEN}$  is implemented as an overriding SET control (active-LOW) to the enable flip-flop.

Scan mode is selected by a HIGH at the SCAN input. Scan input data is shifted in through S\_IN and output data appears at the Q2 output.

All registers are clocked on the positive transition of CLK. Additional lead-frame grounding is provided through the Ground pins (GND) which should be connected to 0V. The GND pins are not electrically connected to the chip.

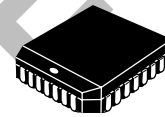
The 100 Series contains temperature compensation.

- Scannable Version of E336
  - 25 Ω Cutoff Bus Outputs
  - 50 Ω Receiver Outputs
  - Scannable Registers
  - Sync. and Async. Bus Enables
  - Non-inverting Data Path
  - 1500 ps Max. Clock to Bus (Data Transmit)
  - 1000 ps Max. Clock to Q (Data Receive)
  - Bus Outputs Feature Internal Edge Slow-Down Capacitors
  - Additional Package Ground Pins
  - PECL Mode Operating Range:  $V_{CC} = 4.2\text{ V to }5.7\text{ V}$  with  $V_{EE} = 0\text{ V}$
  - NECL Mode Operating Range:  $V_{CC} = 0\text{ V}$  with  $V_{EE} = -4.2\text{ V to }-5.7\text{ V}$
  - Internal Input Pulldown Resistors
  - ESD Protection: > 1 KV HBM, > 75 V MM
  - Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
  - Moisture Sensitivity Level 1
- For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 code V-0 @ 1/8", Oxygen Index 28 to 34
  - Transistor Count = 471 devices



ON Semiconductor™

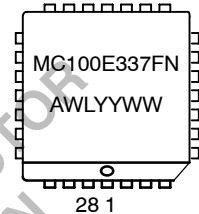
<http://onsemi.com>



PLCC-28  
FN SUFFIX  
CASE 776

A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

### MARKING DIAGRAM



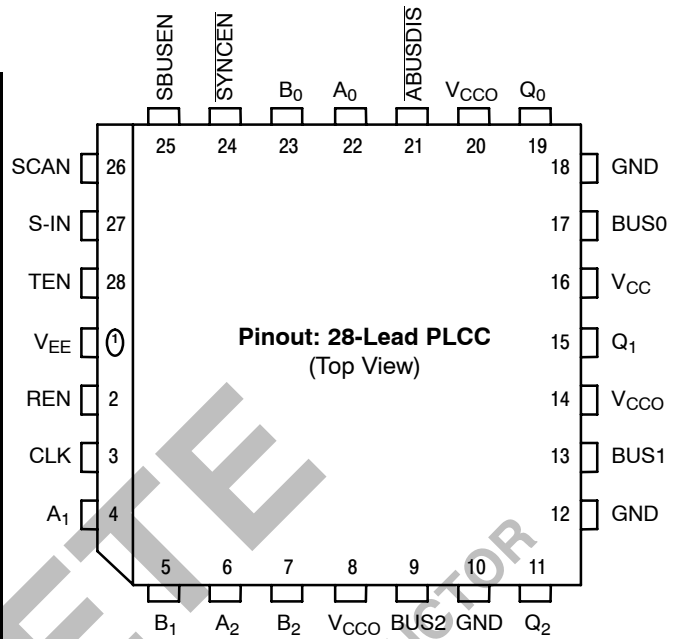
### ORDERING INFORMATION

Device	Package	Shipping
MC100E337FN	PLCC-28	37 Units/Rail
MC100E337FNR2	PLCC-28	500 Units/Reel

# MC100E337

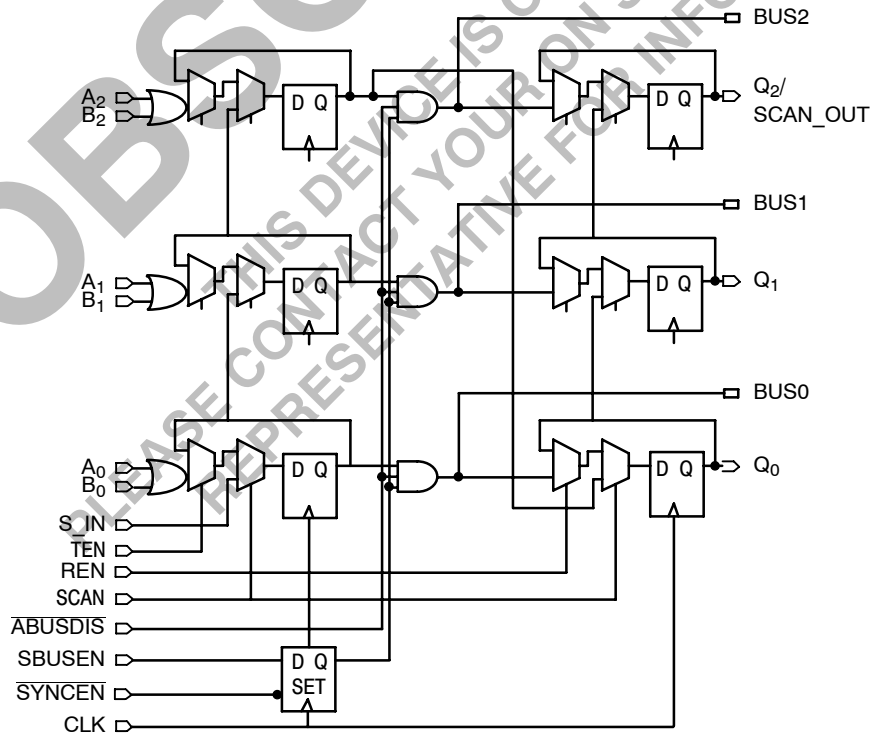
## PIN DESCRIPTION

PIN	FUNCTION
A <sub>0</sub> - A <sub>2</sub>	ECL Data Inputs A
B <sub>0</sub> - B <sub>2</sub>	ECL Data Inputs B
S-IN	ECL Serial (Scan) Data Input
TEN, REN	HOLD/LOAD Controls
SCAN	ECL Scan Control
ABUSDIS	ECL Asynchronous Bus Disable
SBUSEN	ECL Synchronous Bus Enable
SYNCEN	ECL Synchronous Enable Control
CLK	ECL Clock
BUS0 - BUS2	ECL 25Ω Cutoff Bus Outputs
Q <sub>0</sub> - Q <sub>2</sub>	ECL Receive Data Outputs (Q <sub>2</sub> serves as SCAN_OUT in scan mode)
V <sub>CC</sub> , V <sub>CCO</sub>	Positive Supply
V <sub>EE</sub>	Negative Supply
GND	Ground



\* All V<sub>CC</sub> and V<sub>CCO</sub> pins are tied together on the die.  
 Warning: All V<sub>CC</sub>, V<sub>CCO</sub>, and V<sub>EE</sub> pins must be externally connected to Power Supply to guarantee proper operation.

**Figure 1. Pinout Assignment**



**Figure 2. Logic Diagram**

# MC100E337

## MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V <sub>CC</sub>	PECL Mode Power Supply	V <sub>EE</sub> = 0 V		8	V
V <sub>EE</sub>	NECL Mode Power Supply	V <sub>CC</sub> = 0 V		-8	V
V <sub>I</sub>	PECL Mode Input Voltage	V <sub>EE</sub> = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub>	6	V
	NECL Mode Input Voltage	V <sub>CC</sub> = 0 V	V <sub>I</sub> ≥ V <sub>EE</sub>	-6	V
I <sub>out</sub>	Output Current	Continuous Surge		50	mA
				100	mA
T <sub>A</sub>	Operating Temperature Range			0 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 LFPM	28 PLCC	63.5	°C/W
		500 LFPM	28 PLCC	43.5	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	std bd	28 PLCC	22 to 26	°C/W
V <sub>EE</sub>	PECL Operating Range			4.2 to 5.7	V
	NECL Operating Range			-5.7 to -4.2	V
T <sub>sol</sub>	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

## 100E SERIES PECL DC CHARACTERISTICS V<sub>CCx</sub> = 5.0 V; V<sub>EE</sub> = 0.0 V (Note 2)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I <sub>EE</sub>	Power Supply Current		145	174	145	174		167	200		mA
V <sub>OH</sub>	Output HIGH Voltage (Note 3)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V <sub>OL</sub>	Output LOW Voltage (Note 3)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V <sub>IH</sub>	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V <sub>IL</sub>	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
V <sub>CUT</sub>	Cut-off Output Voltage (Note 3)	2.9		2.97	2.9		2.97	2.9		2.97	V
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lpm is maintained.

2. Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary +0.46 V / -0.8 V.

3. Outputs are terminated through a 50 Ω resistor to V<sub>CC</sub> - 2.10 V.

## 100E SERIES NECL DC CHARACTERISTICS V<sub>CCx</sub> = 0.0 V; V<sub>EE</sub> = -5.0 V (Note 4)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I <sub>EE</sub>	Power Supply Current		145	174		145	174		167	200	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 5)	-1025	-950	-880	-1025	-950	-880	-1025	-950	-880	mV
V <sub>OL</sub>	Output LOW Voltage (Note 5)	-1810	-1705	-1620	-1810	-1745	-1620	-1810	-1740	-1620	mV
V <sub>IH</sub>	Input HIGH Voltage	-1165	-950	-880	-1165	-880	-880	-1165	-880	-880	mV
V <sub>IL</sub>	Input LOW Voltage	-1810	-1700	-1475	-1810	-1475	-1475	-1810	-1475	-1475	mV
V <sub>CUT</sub>	Cut-off Output Voltage (Note 5)	2.9		2.97	2.9		2.97	2.9		2.97	V
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lpm is maintained.

4. Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary +0.46 V / -0.8 V.

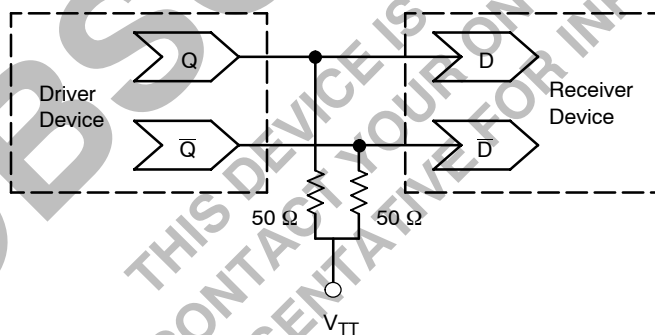
5. Outputs are terminated through a 50 Ω resistor to V<sub>CC</sub> - 2.10 V.

# MC100E337

**AC CHARACTERISTICS**  $V_{CCx} = 5.0\text{ V}; V_{EE} = 0.0\text{ V}$  or  $V_{CCx} = 0.0\text{ V}; V_{EE} = -5.0\text{ V}$  (Note 6)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{MAX}$	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay to Output Clk to Q Clk to BUS $\overline{A}BUSDIS$ SYNCEN	450 800 500 800		1000 1800 1500 1800	450 800 500 800		1000 1800 1500 1800	450 800 500 800		1000 1800 1500 1800	ps
$t_s$	Setup Time BUS SBUSEN Data, S-IN TEN, REN, SCAN	350 100 400 550			350 100 400 550			350 100 400 550			ps
$t_h$	Hold Time BUS SBUSEN Data, S-IN TEN, REN, SCAN	350 500 350 200			350 500 350 200			350 500 350 200			ps
$t_{PW}$	Minimum Pulse Width Clk	400			400			400			ps
$t_{JITTER}$	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
$t_r$ $t_f$	Rise/Fall Times 20 - 80% ( $Q_n$ ) 20 - 80% (BUSn Rise) 20 - 80% (BUSn Fall)	300 500 300		800 1000 800	300 500 300		800 1000 800	300 500 300		800 1000 800	ps

6. 100 Series:  $V_{EE}$  can vary +0.46 V / -0.8 V.



**Typical Termination for Output Driver and Device Evaluation**  
(See Application Note AND8020 – Termination of ECL Logic Devices.)

**Resource Reference of Application Notes**

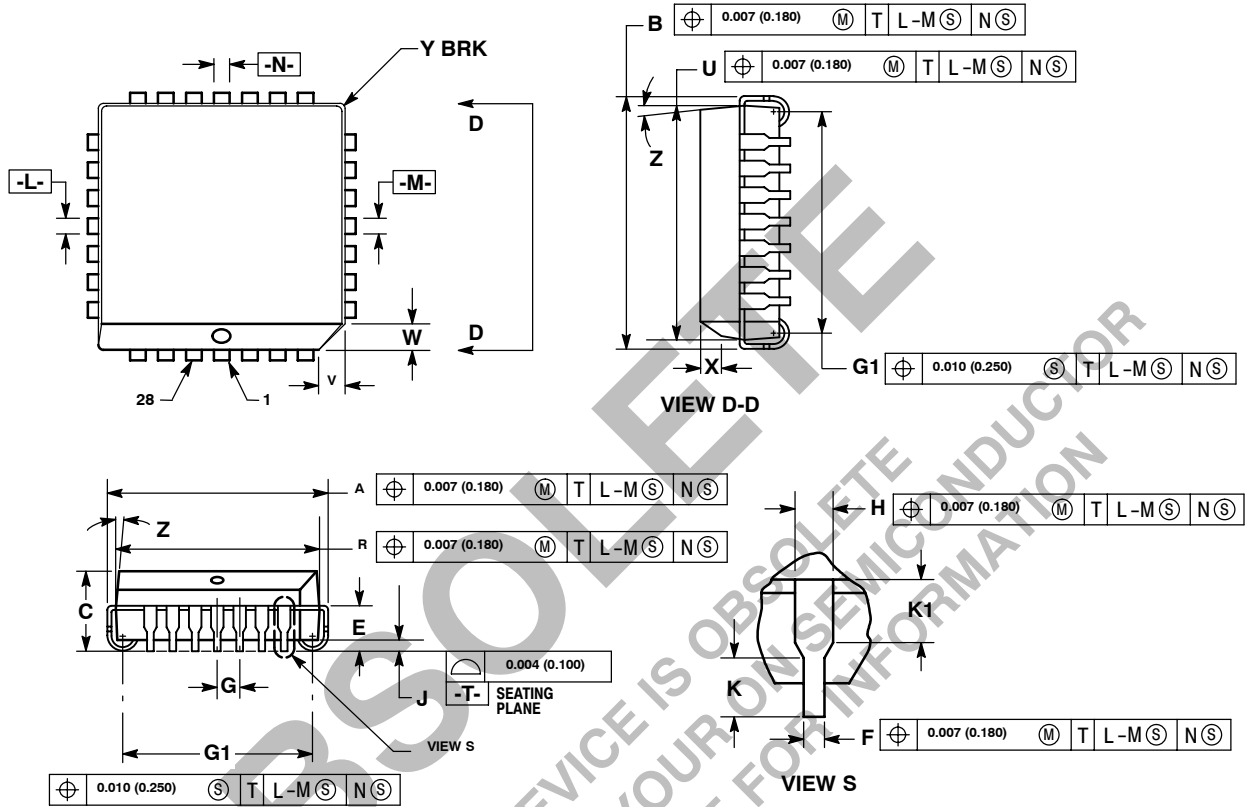
- AN1404** – ECLinPS Circuit Performance at Non-Standard  $V_{IH}$  Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

**OBSOLETE**  
THIS DEVICE IS OBSOLETE  
PLEASE CONTACT YOUR ON SEMICONDUCTOR  
REPRESENTATIVE FOR INFORMATION

# MC100E337

## PACKAGE DIMENSIONS

PLCC-28  
FN SUFFIX  
PLASTIC PLCC PACKAGE  
CASE 776-02  
ISSUE E



**NOTES:**

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

**OBSOLETE**  
 THIS DEVICE IS OBSOLETE  
 PLEASE CONTACT YOUR ON SEMICONDUCTOR  
 REPRESENTATIVE FOR INFORMATION

**ON Semiconductor** and **ON** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

#### PUBLICATION ORDERING INFORMATION

##### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
 P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
 USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
 Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
 Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local  
 Sales Representative